Sheet 1 of 2 sheet(s) Docket No. Serial No. U.S. Department of Commerce, Patent and Trademark Office **UNKNOWN** ROC920010293US1 (PTO Form 1449 modified) LIST OF PATENTS AND PUBLICATIONS CITED BY APPLICANT Applicant Confirmation BERGLUND ET AL. No.: **UNKNOWN** Filing Date Group (Use several sheets if necessary) UNKNOW E Herewith **UNKNOWN** Examiner **U.S. Patent Documents** Filing Date Applicant(s) Class Subclass Issue \*Examiner Document Name Appropriate Number Date Initial 403 11-04-1993 Sims et al. 364 07-18-1995 5,434,775 **A1** 200.53 08-27-1996 395 Malcolm 06-15-1999 **A2** 5,913,034 03-25-1997 10 707 Knoblock et al. **A3** 6,023,699 02-08-2000 224 08-16-1996 709 02-22-2000 Allen et al. **A4** 6,029,199 03-07-1997 709 223 **Taghadoss** 04-18-2000 6,052,722 **A5** 03-25-1997 10 Knoblock et al. 707 01-02-2001 6,169,987 **A6 A7 8A Foreign Patent Documents** Translation Class Subclass Country Date Document \*Examiner YEŜ ' <sup>(\*)</sup> Number 44.44 NO Initial .... X 12/03/1996 Japan JP8320816 **B1** X .... UK 05-04-2000 GB2346463A B<sub>2</sub> OTHER ART Including Author, Title, Date, Pertinent Pages, Etc. \*Examiner Initial DMTF; Network Management and Administration, Winston Bumpus, April 3, 2001 C<sub>1</sub> IButton™ OVERVIEW, Table of Contents, Preface, pp. 1-151 C2 Utilizing the World's Last Expensive Network Topology, Mike Willey, VP Paragon C3 Innovations, Inc.; Embedded Systems Conference West 2001, Class No. 546, pp 1-39 Dallas Semiconductor, Application Note 27, Understanding and Using Cyclic Redundancy C4 Checks with Dallas Semiconductor iButton™ Products , 11-08-99, pp. 1-16 Dallas Semiconductor, Application Note 74, Reading and Writing iButtons via Serial. C5 Interfaces, 02-08-00, pp. 1-39 Dallas Semiconductor; DS1820, 1-Wire™ Digital Thermometer, 030598, pp. 1-27 C6 Dallas Semiconductor; DS2409, MicroLan Coupler, 102199, pp. 1-18 **C7** Dallas Semiconductor; DS2433, 4k-Bit 1-Wire™ EEPROM, 062299, pp. 1-19 **C8** Dallas Semiconductor; DS2450, 1-Wire™ Quad A/D Converter, 012401, pp. 1-24 C9 **Date Considered** Examiner \*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

Sheet 2 of 2 sheet(s) Docket No. Serial No. U.S. Department of Commerce, Patent and Trademark Office **UNKNOWN** ROC920010293US1 (PTO Form 1449 modified) LIST OF PATENTS AND PUBLICATIONS CITED BY APPLICANT Confirmation Applicant BERGLUND ET AL. No.: **UNKNOWN** Group Filing Date (Use several sheets if necessary) UNKNOWN **HEREWITH UNKNOWN** Examiner **U.S. Patent Documents** Subclass Filing Date If Applicant(s) Class Issue \*Examiner Document Name Appropriate Number Date Initial **A1 A2 A3** Α4 **A5** A6 **A7 8A Foreign Patent Documents** Translation Subclass Class Country **Document** Date \*Examiner Number NO Initial YES **B1** B2 **B3 OTHER ART** Including Author, Title, Date, Pertinent Pages, Etc. \*Examiner Initial Dallas Semiconductor; DS2480B, Serial 1-Wire™ Line Driver with Load Sensor, 101999, pp. C10 1-30 Dallas Semiconductor; DS2502, 1 kbit Add-Only Memory, 102199, pp. 1-22 C11 Dallas Semiconductor; DS2502-E64, 1EEE EUI-64 Node Address Chip, 102099, pp. 1-2 C12 Dallas Semiconductor; Dallas Semiconductor; DS2890, 1-Wire™ Digital Potentiometer, C13 061500, pp. 1-27 Dallas Semiconductor; DS9502, ESD Protection Diode, 102199, pp.1-3 C14 Dallas Semiconductor; DS9503m Protection Diode with Resistors, 102199, pp. 1-3

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

Dallas Semiconductor; Tech Brief No. 1, 1-Wire Net Design Guide, 1/21/01, pp. 1-33

**Date Considered** 

C15

C16

Examiner

#2

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Berglund et al.

Serial No.: Unknown

Confirmation No.: Unknown

Filed:

Herewith

For:

**Architecture for Connection** 

and Aggregation of

Components Within a Rack

Group Art Unit: Unknown

Examiner:

Unknown



Assistant Commissioner for Patents Washington, D.C. 20231

Dear Sir:

## **CERTIFICATE UNDER 37 CFR 1.10**

I hereby certify that this correspondence is being deposited on February 13, 2002 with the United States Postal Service in an envelope as "Express Mail Post Office to Addressee," mailing label No. EV041915927US, addressed to: BOX PATENT APPLICATION, Assistant Commissioner for Patents, Washington, D.C. 20231.

February 13, 2002

Date

Keith M. Tackett

## INFORMATION DISCLOSURE STATEMENT

The Applicants, and the Attorney who signs below on the basis of the information supplied by the inventor and the information in his file, submit herewith patents, publications, or other information of which they are aware, which may be material to the examination of this application and in respect of which there may be a duty to disclose in accordance with 37 CFR § 1.56.

While the information submitted in this Information Disclosure Statement may be material pursuant to 37 CFR § 1.56, it is not intended to constitute an admission that any patent, publication, or other information referred to therein is prior art for this invention unless specifically designated as such.

In accordance with 37 CFR § 1.97, this Information Disclosure Statement is not to be construed as a representation that a search has been made or that no other possibly material information as defined under 37 CFR § 1.56(a) exists.

The patents and/or publications submitted herewith are set forth on the attached Form PTO-1449.

Respectfully submitted,

Keith M. Tackett

Registration No. 32,008

MOSER, PATTERSON & SHERIDAN, L.L.P.

3040 Post Oak Blvd., Suite 1500

Houston, TX 77056

Telephone: (713) 623-4844 Facsimile: (713) 623-4846 Attorney for Applicant(s)